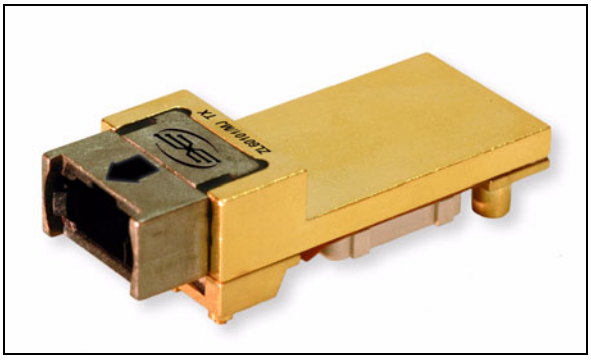
ZARLINK SEMICONDUCTOR

ZL60101 TX / ZL60102 RX

12 x 2.7 Gbps Parallel Fiber Optic Link Transmitter and Receiver

Data Sheet

Issue 1.0 November 2002



Ordering Information

ZL60101/MJD Parallel Fiber Transmitter
ZL60102/MJD Parallel Fiber Receiver

Options

ZL6010*/MKD Module with EMI shield
ZL6010*/MLD Module with external heat sink
ZL6010*/MMD Module with external heat sink and EMI shield

Features

- 12 parallel channels, total 32.6 Gbps capacity
- Data rate up to 2.72 Gbps per channel
- 850 nm VCSEL array
- Data I/O is CML compatible with DC blocking capacitors
- Link reach 300 m with 50/125 μm 500 MHz·km fiber at 2.5 Gbps
- Channel BER better than 10^{-12}
- Industry standard MPO/MTP™ ribbon fiber connector interface
- Pluggable MegArray® ball grid array connector
- Optionally available with EMI shield and external heat sink
- Laser class 1M IEC 60825-1:2001 compliant
- Power supply 3.3 V
- Compatible with industry MSA

Applications

- High-speed interconnects within and between switches, routers and transport equipment
- Proprietary backplanes
- Low cost SONET/SDH VSR (Very Short Reach) OC-192/STM64 connections
- InfiniBand® connections
- Interconnects rack-to-rack, shelf-to-shelf, board-to-board, board-to-optical backplane

Description

The ZL60101 and ZL60102 together make a very high speed transmitter/receiver pair for parallel fiber applications.

The transmitter module converts parallel electrical input signals via a laser driver and a VCSEL array into parallel optical output signals at a wavelength of 850nm.

The receiver module converts parallel optical input signals via a PIN photodiode array and a transimpedance and limiting amplifier into electrical output signals.

The modules are pluggable each fitted with an industry-standard MegArray® BGA connector. This provides ease of assembly on the host board and enables provisioning of bandwidth on demand.

Table of Contents

Features **1**
Applications **1**
Description **1**
Absolute Maximum Ratings **3**
Recommended Operating Conditions **3**
Transmitter Specifications **4**
Transmitter Control and Status Signals 6
Transmitter Control and Status Timing Diagrams 7
Transmitter Pinout Assignments 9
Transmitter Pin Description 9
Receiver Specifications **10**
Receiver Control and Status Signals 11
Receiver Control and Status Timing Diagrams 12
Receiver Pinout Assignments 13
Receiver Pin Description 13
Package Outline **14**
Circuit Board Footprint 18
Heading Frontplate for Panel Accessed Modules 19
Thermal Characteristics **20**
Regulatory Compliance **21**
Eye safety 21
Electrostatic discharge 21
Electrostatic discharge immunity 21
Electromagnetic interference 21
Handling instructions **21**
Cleaning the optical interface 21
ESD handling 21
Link Reach **22**
Link Model Parameters 22
Electrical Interface - Application Examples **23**

Absolute Maximum Ratings

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Table 1 - Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{CC}	-0.3	4.0	V
Differential input voltage amplitude[1]	ΔV		1.2	V
Voltage on any pin	V_{PIN}	-0.3	V_{CC} + 0.3	V
Relative humidity (non-condensing)	M_{OS}	5	95	%
Storage temperature	T_{STG}	-40	100	°C
ESD resistance	V_{ESD}		±1	kV

1. Differential input voltage amplitude is defined as $\Delta V = |DIN+ - DIN-|$.

Recommended Operating Conditions

These parameters apply both to the transmitter and the receiver.

Table 2 - Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power supply voltage	V_{CC}	3.135	3.465	V
Operating case temperature	T_{CASE}	0	80	°C
Signaling rate (per channel)[1]	f_D	1.0	2.72	Gbps
Link distance[2]	LD	2		m
Data I/O DC blocking capacitors[3]	C_{BLK}	100		nF
Power supply noise[4]	V_{NPS}		200	mV_{p-p}

1. Data patterns are to have maximum run lengths and DC balance shifts no worse than that of a Pseudo Random Bit Sequence of length 2^{23}-1 (PRBS-23). Information on lower bit rates is available on request.
2. For maximum distance, see Table 19.
3. For AC-coupling, DC blocking capacitors external to the module with a minimum value of 100 nF is recommended.
4. Power supply noise is defined at the supply side of the recommended filter for all V_{CC} supplies over the frequency range of 500 Hz to 2720 MHz with the recommended power supply filter in place.

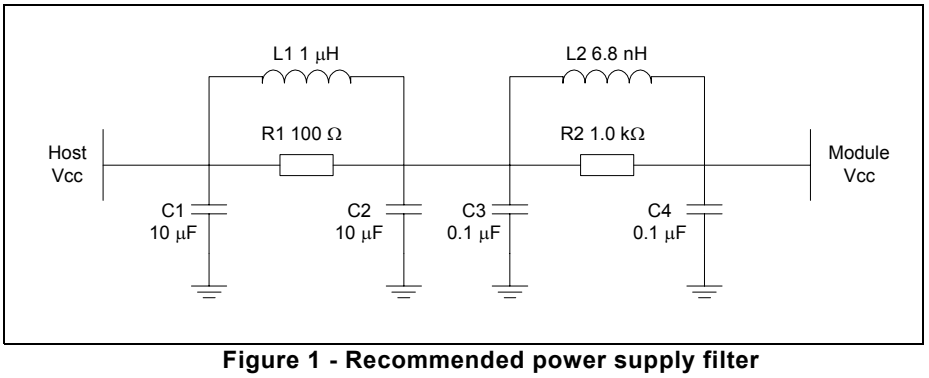


Figure 1 - Recommended power supply filter

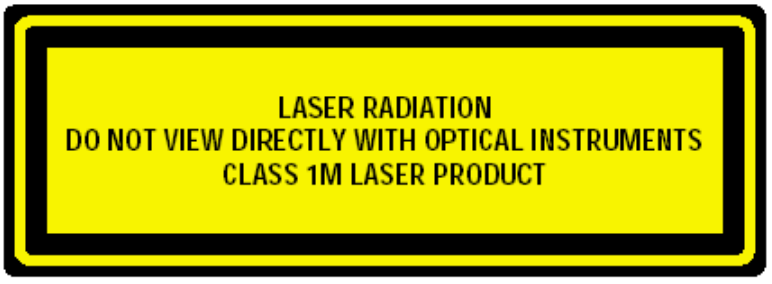
Transmitter Specifications

All parameters below require operating conditions according to Table 2.

Table 3 - Transmitter optical and electrical specifications

Parameter	Symbol	Min	Max	Unit
Optical Parameters				
Launch power (50/125 μm MMF)[1]	P_{OUT}	-7.5	-2	dBm
Extinguished output power	P_{OFF}		-30	dBm
Extinction ratio[2]	ER	7		dB
Optical modulation amplitude[3]	OMA	0.24		mW
Center wavelength	λ_C	830	860	nm
Spectral width[4]	$\Delta\lambda$		0.85	nm_{rms}
Relative intensity noise OMA	$RIN_{12}OMA$		-116	dB/Hz
Optical output rise time (20 - 80%)	t_{RO}		150	ps
Optical output fall time (20 - 80%)	t_{FO}		150	ps
Total jitter contributed (peak to peak)[5]	TJ		120	ps
Deterministic jitter contributed (peak to peak)	DJ		50	ps
Channel to channel skew[6]	t_{SK}		100	ps
Electrical Parameters				
Power dissipation	P_D		1.5	W
Supply current	I_{CC}		450	mA
Differential input voltage amplitude (peak to peak)[7]	ΔV_{IN}	200	1600	mV_{p-p}
Differential input impedance[8]	Z_{IN}	80	120	Ω
Electrical input rise time (20 - 80%)	t_{RE}		160	ps
Electrical input fall time (20 - 80%)	t_{FE}		160	ps

1. The output optical power is compliant with IEC 60825-1 Amendment 2, Class 1M Accessible Emission Limits.
2. The extinction ratio is measured at 622 Mbps.
3. Informative. Corresponds to P_{OUT} = -7.5 dBm and ER = 7 dB.
4. Spectral width is measured as defined in EIA/TIA-455-127 *Spectral Characterization of Multimode Laser Diodes*.
5. Total jitter equals TP1 to TP2 as defined in IEEE 802.3 clauses 38.2 and 38.6 (Gigabit Ethernet).
6. Channel skew is defined for the condition of equal amplitude, zero ps skew signals applied to the transmitter inputs.
7. Differential input voltage is defined as the peak to peak value of the differential voltage between DIN+ and DIN-. Data inputs are CML compatible.
8. Differential input impedance is measured between DIN+ and DIN-.



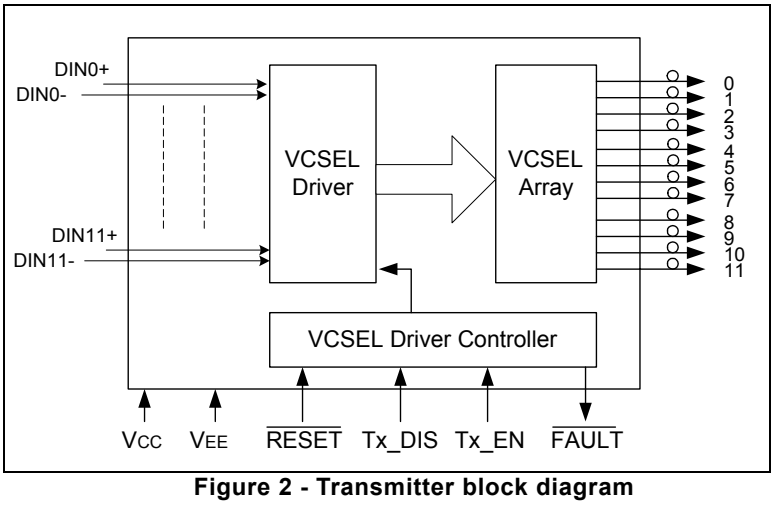


Figure 2 - Transmitter block diagram

Table 4 - Transmitter optical channel assignment

Front view - MTP key up											
Ch 11	Ch 10	Ch 9	Ch 8	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1	Ch 0
Host circuit board											

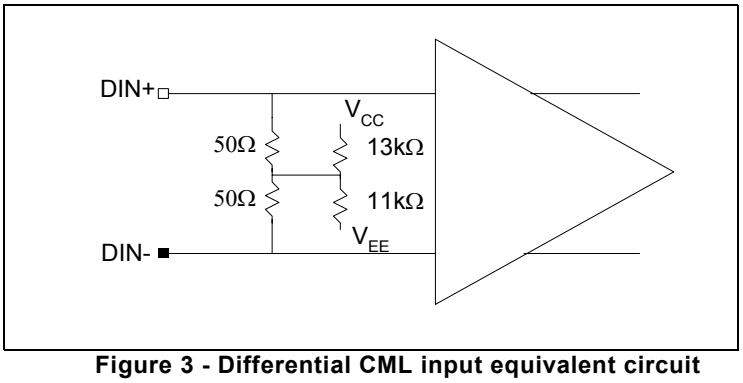


Figure 3 - Differential CML input equivalent circuit

Transmitter Control and Status Signals

The following table shows the timing relationships of the status and control signals of the pluggable optical transmitter.

Table 5 - Transmitter control and status signals

Parameter	Symbol	Min	Typ	Max	Unit
Control input voltage high[1]	V_{IH}	2.1			V
Control input voltage low	V_{IL}			0.62	V
Control pull-up resistor[2]	R_{PU1}		10		kΩ
Control pull-down resistor[3]	R_{PD}		10		kΩ
Status output voltage low[4, 5]	V_{OL}			0.4	V
Status pull-up resistor[4]	R_{PU2}	20		100	kΩ
$\overline{\text{FAULT}}$ assert time	T_{FA}			100	µs
$\overline{\text{FAULT}}$ lasers off	T_{FD}			100	µs
$\overline{\text{RESET}}$ duration	T_{TDD}	10			µs
$\overline{\text{RESET}}$ assert time	T_{OFF}		5	10	µs
$\overline{\text{RESET}}$ de-assert time	T_{ON}			100	ms
Tx_EN assert time	T_{TEN}			1	ms
Tx_EN de-assert time	T_{TD}		5	10	µs
Tx_DIS assert time	T_{TD}		5	10	µs
Tx_DIS de-assert time	T_{TEN}			1	ms

1. Applies to control signals $\overline{\text{RESET}}$, Tx_DIS and Tx_EN.
2. Applies to control signals $\overline{\text{RESET}}$ and Tx_EN. Internal pull-up resistor.
3. Applies to control signal Tx_DIS. Internal pull-down resistor.
4. Applies to status signal $\overline{\text{FAULT}}$. Internal pull-up to V_{CC}.
5. With status output sink current max. 2 mA.

Transmitter Control and Status Timing Diagrams

The following figures show the timing relationships of the status and control signals of the pluggable optical transmitter.

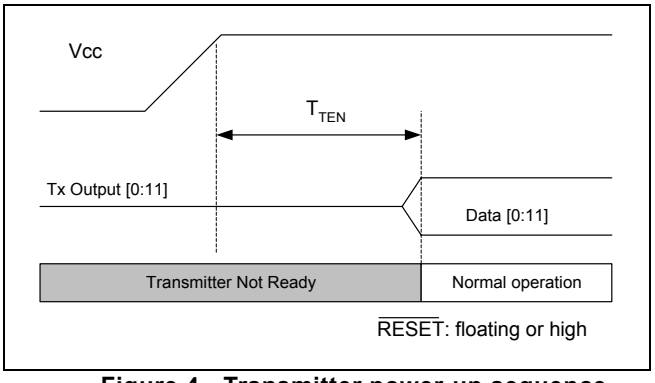


Figure 4 - Transmitter power-up sequence

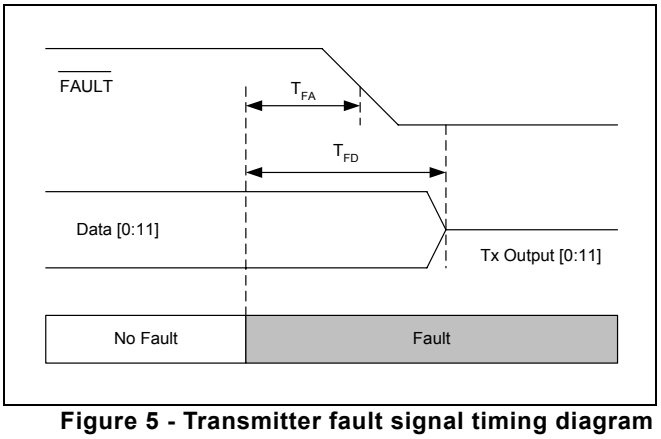


Figure 5 - Transmitter fault signal timing diagram

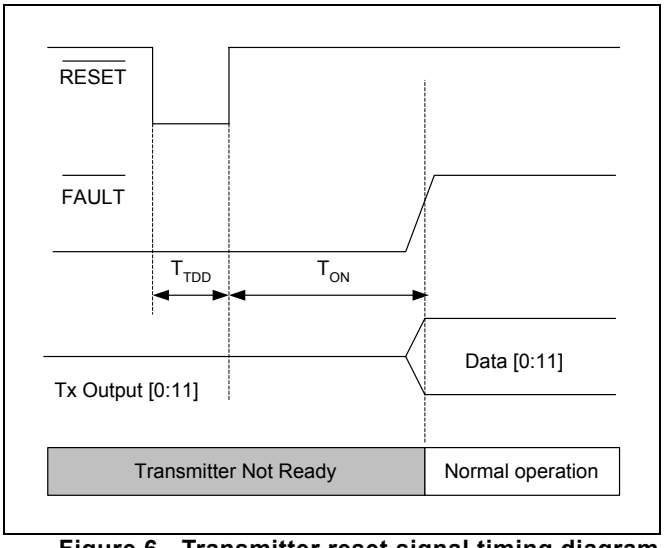


Figure 6 - Transmitter reset signal timing diagram

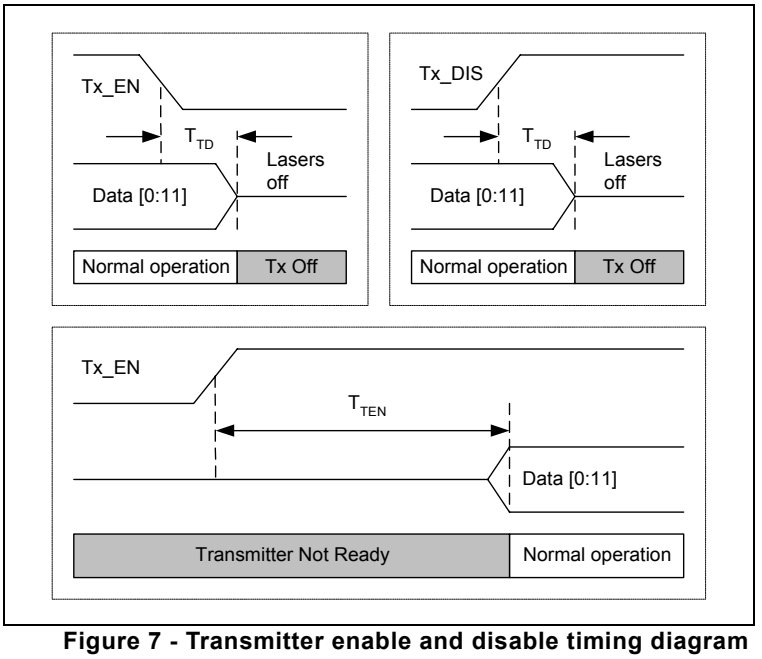


Figure 7 - Transmitter enable and disable timing diagram

Table 6 - Truth table for transmitter operation (Pre-condition: $\overline{\text{RESET}}$ floating or HIGH)

	Tx_DIS High	Tx_DIS Low
Tx_EN High	Transmitter disabled	**Normal operation**
Tx_EN Low	Transmitter disabled	Transmitter disabled

Transmitter Pinout Assignments

Table 7 - Transmitter host circuit board layout (Top view, toward MPO/MTP™ connector end)

	K	J	H	G	F	E	D	C	B	A
1	NIC	NIC	NIC	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	NIC
2	NIC	NIC	NIC	V_{EE}	V_{EE}	DIN5+	V_{EE}	V_{EE}	DIN8+	V_{EE}
3	NIC	V_{CC}	V_{CC}	V_{EE}	DIN4+	DIN5-	V_{EE}	DIN7+	DIN8-	V_{EE}
4	NIC	V_{CC}	V_{CC}	DIN3+	DIN4-	V_{EE}	DIN6+	DIN7-	V_{EE}	NIC
5	NIC	V_{CC}	V_{CC}	DIN3-	V_{EE}	DIN2+	DIN6-	V_{EE}	DIN9-	V_{EE}
6	NIC	V_{CC}	V_{CC}	V_{EE}	DIN1+	DIN2-	V_{EE}	DIN10-	DIN9+	V_{EE}
7	NIC	NIC	NIC	DIN0+	DIN1-	V_{EE}	DIN11-	DIN10+	V_{EE}	NIC
8	DNC	$\overline{\text{RESET}}$	$\overline{\text{FAULT}}$	DIN0-	V_{EE}	V_{EE}	DIN11+	V_{EE}	V_{EE}	NIC
9	DNC	Tx_EN	Tx_DIS	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	NIC
10	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC

(10x10 array, 1.27 mm pitch)

Transmitter Pin Description

Table 8 - Transmitter pin descriptions

Signal Name	Type	Description	Comments
DIN[0:11] +/-	Data input	Transmitter data in, channel 0 to 11	Internal differential termination at 100 Ω.
V_{CC}		Transmitter power supply rail	
V_{EE}		Transmitter signal common. All transmitter voltages are referenced to this potential unless otherwise stated.	Directly connect these pads to the PC board transmitter signal ground plane.
Tx_EN	Control input	Transmitter enable. HIGH: normal operation LOW: disable transmitter	Active high, internal pull-up. See Table 6.
Tx_DIS	Control input	Transmitter disable. HIGH: disable transmitter LOW: normal operation	Active high, internal pull-down. See Table 6.
$\overline{\text{FAULT}}$	Status output	Transmitter fault. HIGH: normal operation LOW: laser fault detected on at least one channel	When active, all channels are disabled. Clear by reset signal. Internal pull-up.
$\overline{\text{RESET}}$	Control input	Transmitter reset. HIGH: normal operation LOW:reset to clear fault signal	Internal pull-up.
DNC		Do not connect to any potential, including ground.	
NIC		No internal connection.	

Receiver Specifications

All parameters below require operating conditions according to Table 2 and a termination load of 100 Ω differential at the electrical output.

Table 9 - Receiver optical and electrical parameters

Parameter	Symbol	Min	Max	Unit
Optical Parameters				
Input optical power[1]	P_{IN}	-16	-2	dBm
Center wavelength	λ_C	830	860	nm
Return loss[2]	RL	12		dB
Total jitter contributed (peak to peak)[3]	TJ		120	ps
Deterministic jitter contributed (peak to peak)	DJ		50	ps
Stressed receiver sensitivity[4]	P_{SS}		-11.3	dBm
Channel to channel skew[5]	t_{SK}		100	ps
Signal detect assert	P_{SA}		-17	dBm
Signal detect de-assert	P_{SD}	-27		dBm
Electrical Parameters				
Power dissipation	P_D		1.5	W
Supply current	I_{CC}		450	mA
Differential output voltage amplitude (peak to peak)[6]	ΔV_{OUT}	500	800	mV_{p-p}
Output differential load impedance[7]	Z_L	80	120	Ω
Stressed receiver eye opening[8]	P_{SE}	0.3		UI
Electrical output rise time (20 - 80 %)	t_{RE}		150	ps
Electrical output fall time (20 - 80 %)	t_{FE}		150	ps

1. Receive power for a channel is measured for a BER of 10^{-12} and worst case extinction ratio. P_{IN} (Min) is measured using a fast rise/fall time source with low RIN and adjacent channel(s) operating with with incident power of 6 dB above P_{IN} (Min).
2. Return loss is measured as defined in TIA/EIA-455-107A *Determination of Component Reflectance or Link/System Return Loss Using a Loss Test Set.*
3. Total jitter equals TP3 to TP4 as defined in IEEE 802.3 clauses 38.2 and 38.6 (Gigabit Ethernet).
4. The stressed receiver sensitivity is measured using PRBS 2^{23}-1 pattern, 2.7 dB inter-symbol interference, ISI (Min), 30 ps duty cycle dependent deterministic jitter, DCD DJ (Min), and 7 dB extinction ratio, ER (Min) (ER penalty = 1.76 dB). All channels not under test are receiving signals with an average input power of 6 dB above P_{IN} (Min).
5. Channel skew is defined for the condition of equal amplitude, zero ps skew signals applied to the receiver inputs.
6. Differential output voltage is defined as the peak to peak value of the differential voltage between DOUT+ and DOUT- and measured with a 100 Ω differential load connected between DOUT+ and DOUT-. Data outputs are CML compatible.
7. See Figure 19.
8. The stressed receiver eye opening represents the eye at TP4 as defined in IEEE 802.3 clauses 38.2 and 38.6 (Gigabit Ethernet). The stressed receiver eye opening is measured using PRBS 2^{23}-1 pattern, 2.7 dB ISI min, 30 ps DCD DJ min, 7 dB ER min and an average input power of -10.8 dBm (0.5 dB above minimum stressed receiver sensitivity as defined in IEEE 802.3 clause 38.6). All channels not under test are receiving signals with an average input power of 6 dB above P_{IN} (Min).

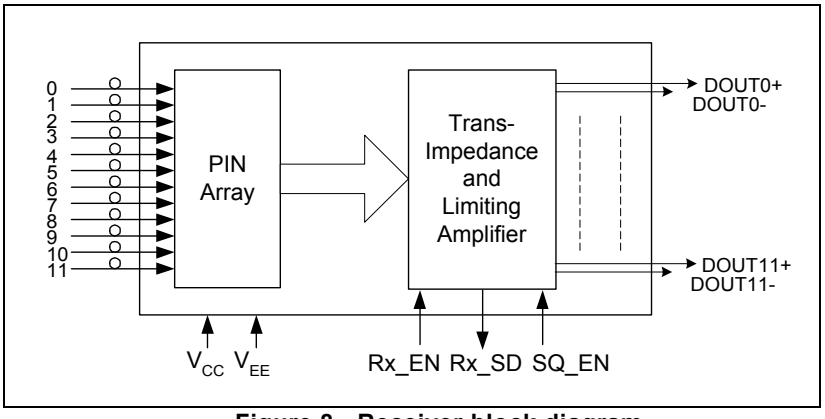


Figure 8 - Receiver block diagram

Table 10 - Receiver optical channel assignment

Front view - MTP key up											
Ch 11	Ch 10	Ch 9	Ch 8	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1	Ch 0
Host circuit board											

Receiver Control and Status Signals

The following table shows the timing relationships of the status and control signals of the pluggable optical receiver.

Table 11 - Receiver control and status signals

Parameter	Symbol	Min	Typ	Max	Unit
Control input voltage high[1]	V_{IH}	2.0			V
Control input voltage low[1]	V_{IL}			0.9	V
Control input pull-up current[1]	$\lvert I_{IN} \rvert$	10		100	µA
Status output voltage low[2, 3]	V_{OL}			0.4	V
Status output pull-up resistor[2]	R_{PU}		3.25		kΩ
Receiver signal detect assert time	T_{SD}		50	200	µs
Receiver signal detect de-assert time	T_{LOS}		50	200	µs
Receiver enable assert time	T_{RXEN}		33		ms
Receiver enable de-assert time	T_{RXD}		5		µs

1. Applies to control signals Rx_EN, SQ_EN.
2. Applies to status signal Rx_SD. Internal pull-up to V_{CC}.
3. With status output sink current max 2 mA.

Receiver Control and Status Timing Diagrams

The following figures show the timing relationships of the status and control signals of the pluggable optical receiver.

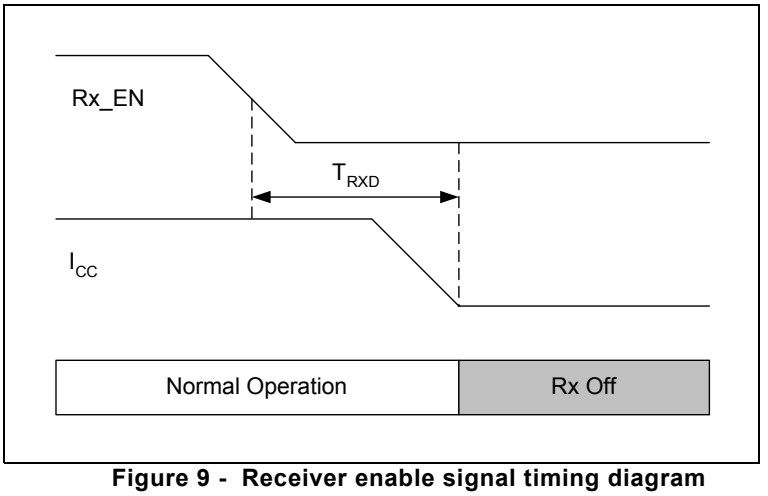


Figure 9 - Receiver enable signal timing diagram

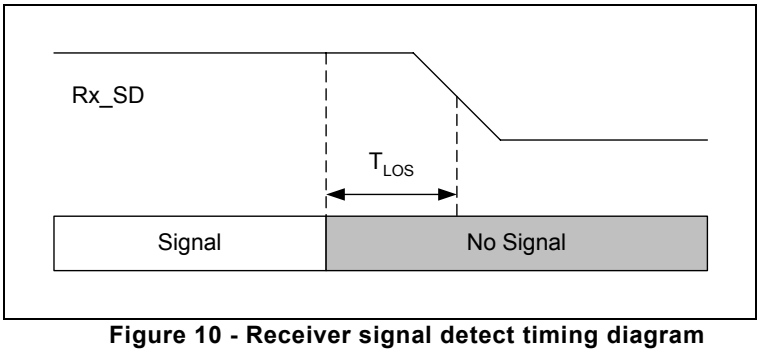


Figure 10 - Receiver signal detect timing diagram

Receiver Pinout Assignments

Table 12 - Receiver pinout assignments (Top view, toward MPO/MTP™ connector end)

	K	J	H	G	F	E	D	C	B	A
1	DNC	NIC	NIC	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	NIC
2	DNC	NIC	NIC	V_{EE}	V_{EE}	DOUT5-	V_{EE}	V_{EE}	DOUT8-	V_{EE}
3	NIC	V_{CC}	V_{CC}	V_{EE}	DOUT4-	DOUT5+	V_{EE}	DOUT7-	DOUT8+	V_{EE}
4	NIC	V_{CC}	V_{CC}	DOUT3-	DOUT4+	V_{EE}	DOUT6-	DOUT7+	V_{EE}	NIC
5	NIC	V_{CC}	V_{CC}	DOUT3+	V_{EE}	DOUT2-	DOUT6+	V_{EE}	DOUT9+	V_{EE}
6	NIC	V_{CC}	V_{CC}	V_{EE}	DOUT1-	DOUT2+	V_{EE}	DOUT10+	DOUT9-	V_{EE}
7	NIC	NIC	Rx_SD	DOUT0-	DOUT1+	V_{EE}	DOUT11+	DOUT10-	V_{EE}	NIC
8	DNC	NIC	NIC	DOUT0+	V_{EE}	V_{EE}	DOUT11-	V_{EE}	V_{EE}	NIC
9	DNC	Rx_EN	NIC	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	NIC
10	SQ_EN	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC

(10x10 array, 1.27 mm pitch)

Receiver Pin Description

Table 13 - Receiver pin descriptions

Signal Name	Type	Description	Comments
DOUT[0:11] +/-	Data output	Receiver data out, channel 0 to 11.	
V_{CC}		Receiver power supply rail.	
V_{EE}		Receiver signal common. All receiver voltages are referenced to this potential unless otherwise stated.	Directly connect these pads to the PC board transmitter signal ground plane.
Rx_EN	Control input	Receiver enable. HIGH: normal operation LOW: disable receiver	Internal pull-up.
Rx_SD	Status output	Receiver signal detect. HIGH: valid optical input on all channels LOW: loss of signal on at least one channel	Internal pull-up.
SQ_EN	Control input	Squelch enable. HIGH: squelch function enabled. Data OUT is squelched on any channels that have loss of signal LOW: squelch function disabled	Internal pull-up.
DNC		Do not connect to any potential, including ground.	
NIC		No internal connection.	

Package Outline

Tolerancing per ASME Y14.5M-1994. All dimensions are in millimeters.

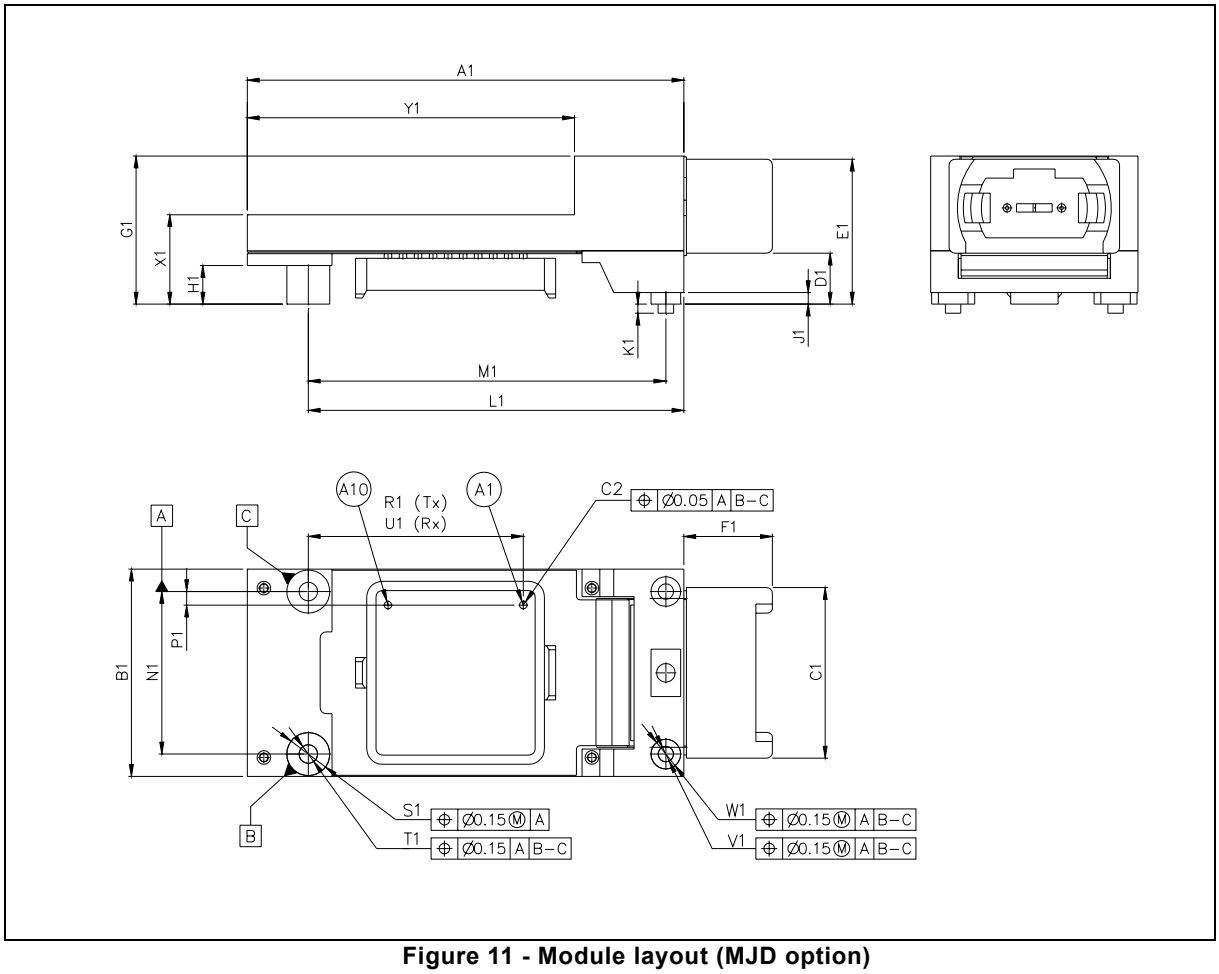


Figure 11 - Module layout (MJD option)

Table 14 - Module dimensions (MJD option)

Key	Dimension [mm]	Comments
A1	36.87	Length of module body, less optical receptacle assembly
B1	17.50	Width of module body
C1	14.40	Width of optical receptacle assembly
D1	4.30	Height of bottom of optical receptacle assembly
E1	12.23	Height of top of optical receptacle assembly
F1	7.48	Length of optical receptacle assembly
G1	12.50	Height of top of module
H1	3.26	Clearance over host board at rear of module
J1	0.98	Height of standoff boss on front posts
K1	0.76	Height of front posts
L1	31.75	Distance from rear post to front plane, less optical receptacle assembly
M1	30.23	Distance from front to rear posts
N1	13.72	Distance between posts, side to side
P1	1.145	Location of BGA pin A1
R1	19.43	Location of BGA pin A1, transmitter
S1	Ø3.63	Diameter of rear posts
T1	2-56 UNC-2B	Thread dimension, minimum 3.50 mm deep
U1	16.89	Location of BGA pin A1, receiver
V1	Ø1.30	Diameter of front posts
W1	Ø2.50	Diameter of standoff boss on front post
X1	7.55	Height of back of module without heat sink
Y1	27.64	Length of external heat sink body

Dimensions with reference designators ending in "2" (e.g., C2) are defined in Table 17.

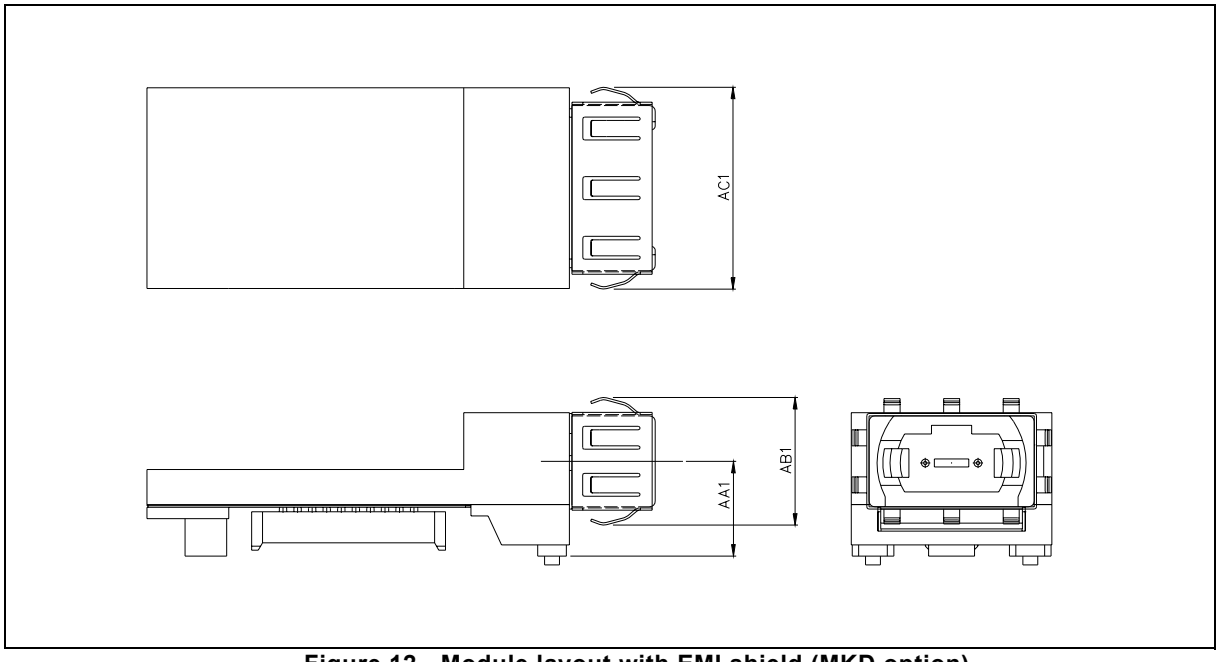


Figure 12 - Module layout with EMI shield (MKD option)

Table 15 - Module dimensions with EMI shield (MKD option)

Key	Dimension [mm]		Comments
	Min	Max	
AA1	8.27		Distance from hostboard to centre of EMI shield
AB1	9.10	11.10	Height of EMI shield with bezel in A2 location
AC1	15.50	17.50	Width of EMI shield with bezel in A2 location

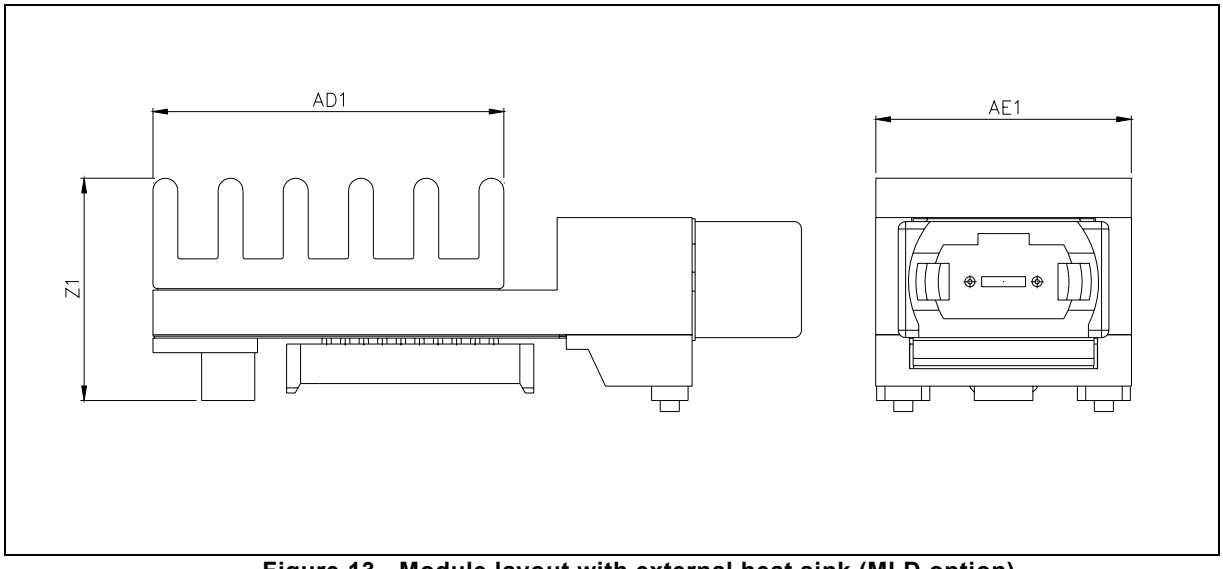


Figure 13 - Module layout with external heat sink (MLD option)

Table 16 - Module dimensions with external heat sink (MLD option)

Key	Dimension [mm]	Comments
Z1	15.19	Height of top of module, including external heat sink
AD1	24.00	Length of external heat sink
AE1	17.45	Width of external heat sink

Circuit Board Footprint

Tolerancing per ASME Y14.5M-1994. All dimensions are in millimeters.

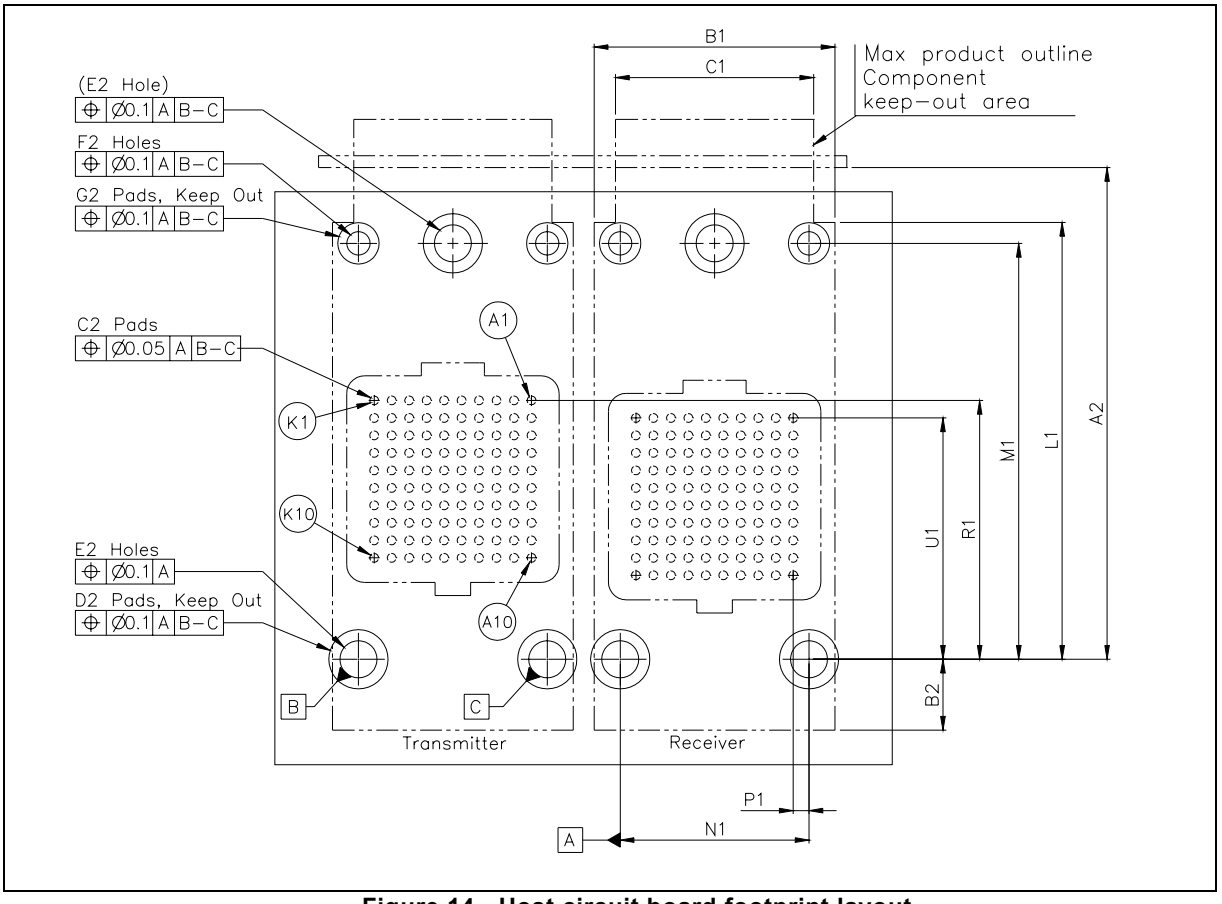


Figure 14 - Host circuit board footprint layout

Table 17 - Host circuit board footprint dimensions

Key	Dimension [mm]	Tolerance [mm]	Comments
A2	35.31	±0.75	Distance from rear post to inside surface of bezel
B2	5.15	±0.25	Distance from rear post to rear of module keep-out area
C2	Ø0.58	±0.05	Diameter of pad in BGA pattern
D2	Ø4.50	MIN	Diameter of keep-out pad for rear posts: two rear and one front
E2	Ø2.69	±0.12	Diameter of hole for mounting screws: two rear and one front
F2	Ø1.70	±0.12	Diameter of hole for front posts
G2	Ø3.30	MIN	Diameter of keep-out pad for front post

Dimensions with reference designators ending in "1" (e.g., B1, C1) are defined in Table 14.

Heading Frontplate for Panel Accessed Modules

Tolerancing per ASME Y14.5M-1994. All dimensions are in millimeters.

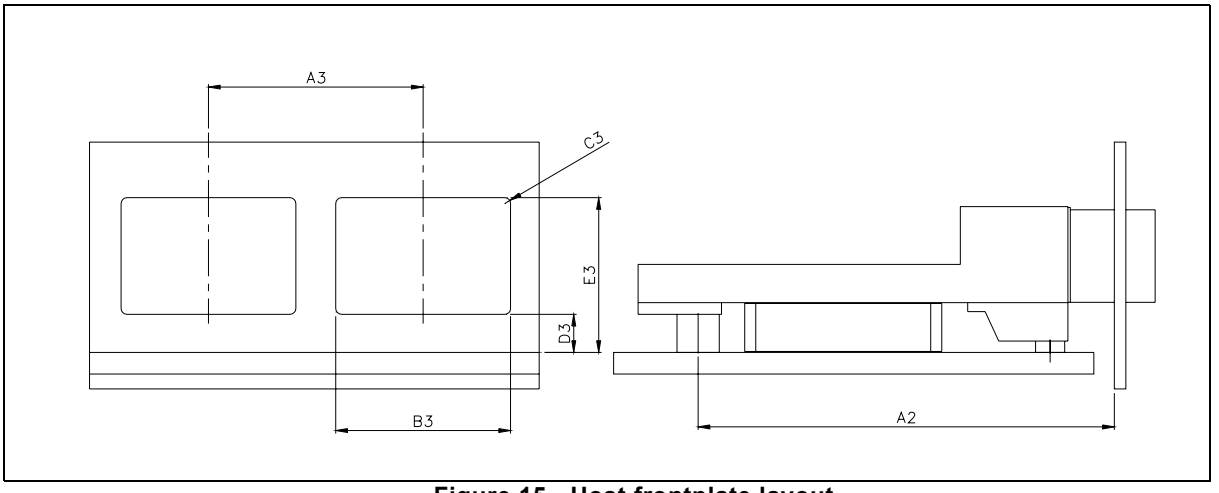


Figure 15 - Host frontplate layout

Table 18 - Host frontplate dimensions

Key	Dimension [mm]	Tolerance [mm]	Comments
A3	18.42	MIN	Centre-to-centre spacing for adjacent modules
B3	16.50	±0.20	Width of opening in frontplate
C3	0.50	MAX	Corner radius of opening in frontplate
D3	3.20	±0.20	Height from host PCB to bottom of frontplate opening
E3	13.33	±0.20	Height from host PCB to top of frontplate opening

Dimensions with reference designators ending in "2" (e.g., A2) are defined in Table 17.

Thermal Characteristics

There are three options for heat sinks depending on the cooling needs. They are

1. Direct application without any attached external heat sink
2. Use the generic heat sink specified in this data sheet
3. Use a customer designed external heat sink

In Figure 16 and Figure 17, the temperature rise and thermal resistance as a function of air velocity (free air velocity at the top of the module) is shown for option 1 and 2. The thermal resistance is defined as the temperature difference between the case temperature and ambient flowing air divided by the total heat dissipation of the module.

Improved thermal properties can be achieved by using a larger heat sink especially if more height is available (option 3). For this option, a more detailed discussion with Zarlink is recommended regarding heat sink design attachment materials.

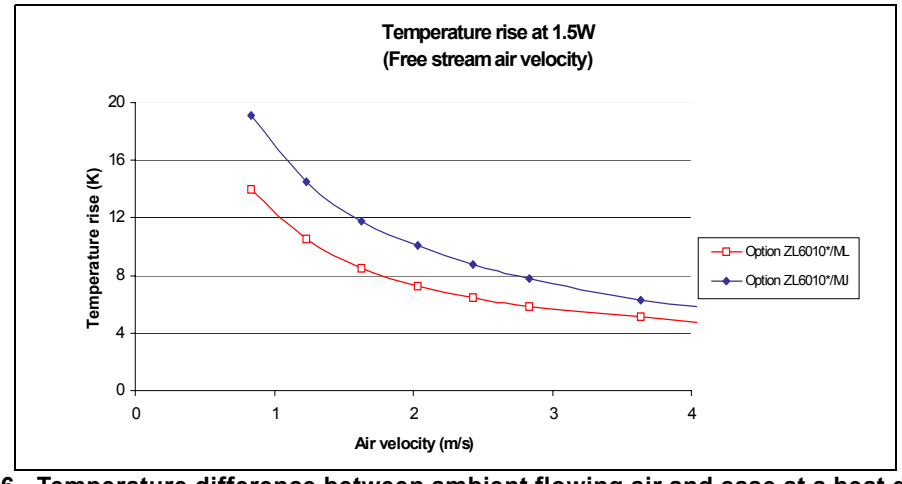


Figure 16 - Temperature difference between ambient flowing air and case at a heat dissipation of 1.5 W

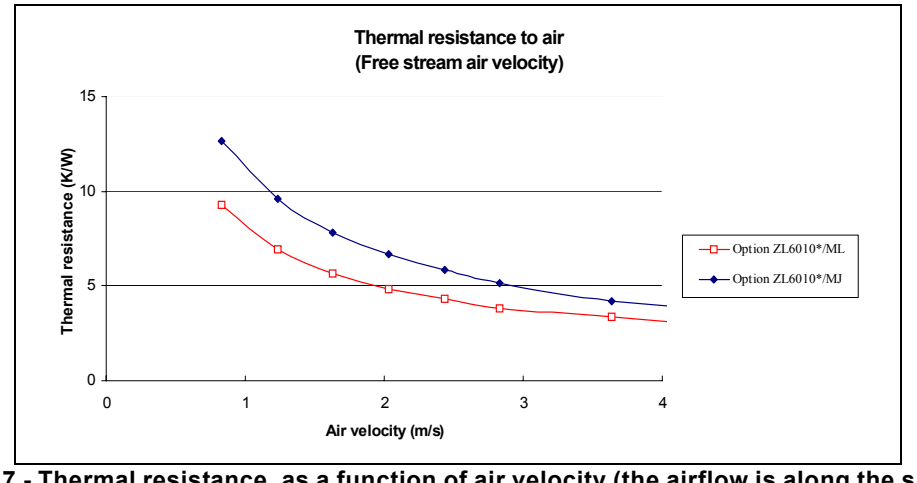


Figure 17 - Thermal resistance, as a function of air velocity (the airflow is along the shortest side of the module). For any other orientation, the thermal resistance is 75-100% of the values shown above

Regulatory Compliance

Eye safety

The maximum optical output power is specified to comply with Class 1M in accordance with IEC 60825−1:2001. In addition the transmitter complies with FDA performance standards for laser products except for deviations pursuant to Laser Notice No.50, dated July 26, 2001. No maintenance or service of the product may be performed.

Electrostatic discharge

The module is classified as Class 1 (> 1000 Volts) according to MIL−STD−883, test method 3015.7, with regards to the electrical pads.

Electrostatic discharge immunity

The part withstand a 15 kV (air discharge) and 8 kV (contact discharge) either indirect or directly to receptacle; tested according to IEC 61000−4−2, while in operation without addition of bit errors.

Electromagnetic interference

Emission

The electromagnetic emission is tested in front of the module (module fitted with EMI shield), with the module mounted in a frontplate cutout as defined in Figure 15. The part is tested with FCC Part 15, 30 − 1000 MHz and 1 GHz to 5th harmonic of the highest fundamental frequency (6.75 GHz), and is specified to be Class B with > 6 dB margin.

Immunity

The electromagnetic immunity is tested without a front panel or enclosure. The module specification is maintained with an applied field of 10 V/m for frequencies between 10 kHz and 10 GHz, according to IEC 61000−4−3 and GR−1089−CORE.

Handling instructions

Cleaning the optical interface

A protective connector plug is supplied with each module. This plug should remain in place prior to use, and be re-attached whenever a fiber cable is not inserted. This will keep the optical interface free from dust or other contaminants, which may potentially degrade the optical signal. Before reattaching the connector plug to the module, visually inspect the plug and remove any contamination. If the optical interface becomes contaminated, it can be cleaned with high-pressure nitrogen.

The use of fluids, or physical contact with the optical interface, is not advised due to potential for damage.

ESD handling

When handling the modules, precautions for ESD sensitive devices should be taken. These include use of ESD protected work areas with wrist straps, controlled work-benches, floors etc.

Link Reach

The following table lists the minimum reach distance of the 12 channel pluggable optical modules for different multi-mode fiber (MMF) types and bandwidths assuming worst case parameters. Each case allows for a maximum of 2 dB per channel connection loss for patch cables and other connectors.

Table 19 - Link reach for different fiber types and data rates

Fiber Type [core / cladding μm]	**Modal Bandwidth @ 850 nm** [MHz*km]	**Reach Distance @ 1 Gbps** [m]	**Reach Distance @ 2.5 Gbps** [m]	**Reach Distance @ 2.72 Gbps** [m]
62.5/125 MMF	200	350	130	110
62.5/125 or 50/125 MMF	400	650	260	220
50/125 MMF	500	750	300	270

Link Model Parameters

The link reaches above have been calculated using the following link model parameters and Gigabit Ethernet link model version 2.3.5 (filename: 5pmd047.xls).

Table 20 - Link model parameters

Parameter	**Symbol**	**Value**	**Unit**
Mode partition noise k-factor	k	0.3	
Modal noise	MN	0.3	dB
Dispersion slope parameter	S_O	0.11	ps/nm^2*km
Wavelength of zero dispersion	U_O	1320	nm
Attenuation coefficient at 850 nm	α_{dB}	3.5	dB/km
Conversion factor	C1	480	ns.MHz
Q-factor [BER 10^{-12}]	Q	7.04	
TP4 eye opening		0.3	UI
DCD allocation at TP3	DCD DJ	0.08	UI
RMS baseline wander S.D.	σ_{BLW}	0.025	
RIN coefficient	k_{RIN}	0.70	
Conversion factor	c_rx	329	ns.MHz

Electrical Interface - Application Examples

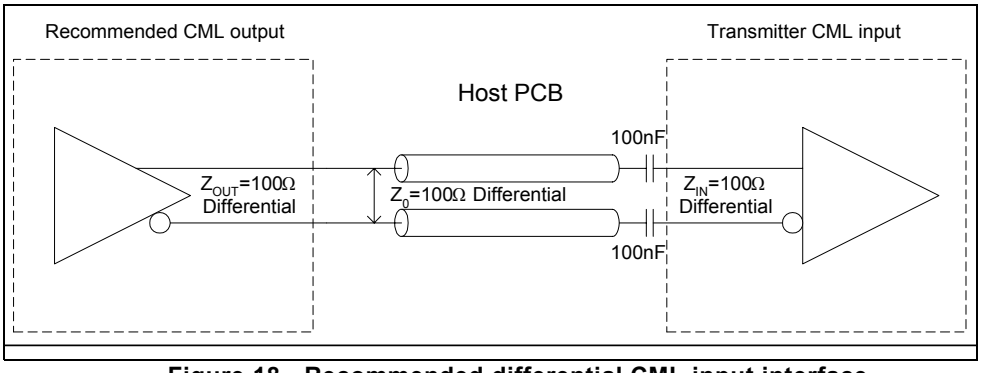


Figure 18 - Recommended differential CML input interface

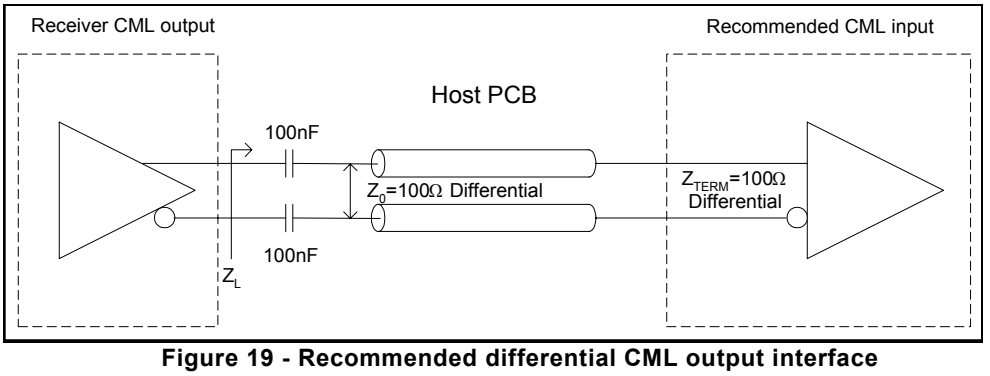


Figure 19 - Recommended differential CML output interface

For more information about all Zarlink products visit our Web Site at

www.zarlink.com